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Form 1449*

**INFORMATION DISCLOSURE STATEMENT
BY APPLICANT**
(Use several sheets if necessary)

Atty. Docket No.: 499.081US1

Applicant: Mark Ronald Sikkink et al.

Filing Date: July 20, 2000

Serial No. 09/621,315

Group: 2664

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U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	4,477,713	10/16/1984	Cook, G.E., et al.	219	124.34	07/09/82
	4,514,749	04/30/1985	Shoji, M.	357	68	01/18/83
	4,587,445	05/06/1986	Kanuma, A.	307	443	05/16/84
	4,823,184	04/18/1989	Belmares-Sarabia, et al.	358	27	09/08/87
	4,926,066	05/15/1990	Maini, R., et al.	307	303.1	09/12/88
	5,295,132	03/15/1994	Hashimoto, K., et al.	370	13	08/25/92
	5,315,175	05/24/1994	Langner, P.A.	307	443	03/18/93
	5,416,606	05/16/1995	Katayama, A., et al.	358	467	09/23/94
	5,481,567	01/02/1996	Betts, W.L., et al.	375	261	09/12/94
	5,544,203	08/06/1996	Casasanta, J.A., et al.	375	376	10/18/94
	5,604,450	02/18/1997	Borkar, S., et al.	326	82	07/27/95
	5,657,346	08/12/1997	Lordi, A.L., et al.	375	224	10/13/95
	5,793,259	08/11/1998	Chengson, D.	331	78	06/20/97
	5,811,997	09/22/1998	Chengson, D.P., et al.	327	112	04/26/96
	5,844,954	12/01/1998	Casasanta, J.A., et al.	375	373	02/20/97
	5,847,592	12/08/1998	Gleim, G., et al.	327	403	09/13/94
	5,898,729	04/27/1999	Boezen, H., et al.	375	259	10/10/95
	6,005,895	12/21/1999	Perino, D.V., et al.	375	288	12/20/96

FOREIGN PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes	No

OTHER DOCUMENTS
(Including Author, Title, Date, Pertinent Pages, Etc.)

**Examiner Initial	
	"Low Power Quad Differential Line Driver with Cut-Off", National Semiconductor, F100K ECL 300 Series Databook and Design Guide, pp. 2-54 - 2-60, (1992)
	"The SA27 library includes programmable delay elements DELAYMUXO and DELAYMUXN. How are these cells used?", IBM Delaymuxn Book, pp. 1-6, (February 1999)
	Djordjevic, A.R., et al., "Time Domain Response of Multiconductor Transmission Lines", Proceedings of the IEEE, 75(6), 743-64, (June 1987)
	Im, G., et al., "Bandwidth-Efficient Digital Transmission over Unshielded Twisted-Pair Wiring", IEEE Journal on Selected Areas in Communications, 13(9), 1643-1655, (December 1995)

Examiner _Danul Hyman_

Date Considered _3 December 2003_

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
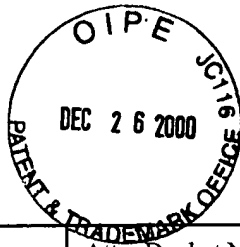
Form 1449*	Atty. Docket No.: 499.081US1	Serial No. 09/621,315
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	Filing Date: July 20, 2000	Group: 2664

OTHER DOCUMENTS
(Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Initial

DJR	Mooney, R., et al., "A 900 Mb/s Bidirectional Signaling Scheme", IEEE Journal of Solid-State Circuits, 30(12), 1538-1543, (Dec. 1995)
DJR	Takahashi, T., et al., "110GB/s Simultaneous Bi-Directional Transceiver Logic Synchronized with a System Clock", IEEE International Solid-State Circuits Conference, 176-177, (1999)

Examiner _Daniel Ryman_ | Date Considered _3 December 2003_

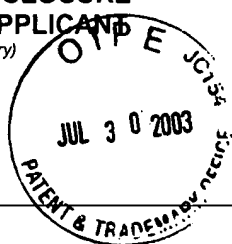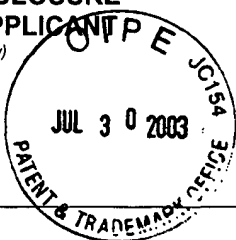*Substitute Disclosure Statement Form (PTO-1449)

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(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known

Application Number	09/621,315
Filing Date	July 20, 2000
First Named Inventor	Sikkink, Mark
Group Art Unit	2731
Examiner Name	Unknown

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US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
DℑZ	US-4,375,051	02/22/1983	Theall, C. E.	333	17	02/19/1981
ℑℛ	US-4,637,018	01/13/1987	Flora, L. P., et al.	371	1	08/29/1984
DℑR	US-4,696,019	09/22/1987	Tulpule, B. R., et al.	375	107	09/19/1984
ℑℛ	US-4,755,704	07/05/1988	Flora, L. P., et al.	307	269	06/30/1987
ℑℛ	US-4,805,195	02/14/1989	Keegan, T. J.	375	106	12/10/1986
ℑℛ	US-4,833,695	05/23/1989	Greub, H. J.	375	118	09/08/1987
DℑR	US-4,845,390	07/04/1989	Chan, S. S.	307	602	01/11/1988
ℑℛ	US-4,860,322	08/22/1989	Lloyd, S. G.	375	107	10/05/1988
ℑℛ	US-4,959,540	09/25/1990	Fan, B. , et al.	250	227.12	05/15/1989
DℑR	US-5,087,829	02/11/1992	Ishibashi, K. , et al.	307	269	12/01/1989
Dℑℛ	US-5,194,765	03/16/1993	Dunlop, Alfred E., et al.	307	443	06/28/1991
DℑR	US-5,287,359	02/15/1994	Engelse, Willem	370	100.1	04/08/1991
Dℑℛ	US-5,329,188	07/12/1994	Sikkink, M. R., et al.	307	517	12/09/1991
Dℑℙ	US-5,394,528	02/28/1995	Kobayashi, Souichi , et al.	395	325	09/02/1992
DℑR	US-5,490,252	02/06/1996	Macera, Mario , et al.	395	200.1	09/30/1992
Dℑℛ	US-5,502,733	03/26/1996	Kishi, T. , et al.	714	748	03/02/1994
Dℑℛ	US-5,506,953	04/09/1996	Dao, Giang	395	166	12/22/1994
DℑR	US-5,603,056	02/11/1997	Totani, Tokuyuki	395	828	09/09/1994
Dℑℛ	US-5,617,537	04/01/1997	Yamada, S. , et al.	395	200.01	10/03/1994
Dℑℛ	US-5,631,611	05/20/1997	Luu, Ky , et al.	333	17.3	06/18/1996
Dℑℙ	US-5,682,512	10/28/1997	Tetrick, R.	395	412	06/30/1995
DℑR	US-5,748,547	05/05/1998	Shau, J-J	365	222	05/24/1996
Dℑℛ	US-5,778,308	07/07/1998	Sroka, Peter , et al.	455	115	12/26/1996
Dℑℛ	US-5,778,429	07/07/1998	Sukegawa, N. , et al.	711	129	07/03/1995
bℑℛ	US-5,784,706	07/21/1998	Oberlin, Steven , et al.	711	202	12/13/1993
DℑR	US-5,828,833	10/27/1998	Belville, Daniel R., et al.	395	187.01	08/15/1996
DℑR	US-5,850,422	12/15/1998	Chen, Dao-Long	375	371	07/21/1995
ℑℛ	US-5,915,104	06/22/1999	Miller, S. C.	395	309	01/09/1997
Dℑℛ	US-5,929,717	07/27/1999	Richardson, Brett C., et al.	333	017.3	01/09/1998
DℑR	US-5,978,953	11/02/1999	Olarig, S. P.	714	768	12/19/1996
ℑℛ	US-6,016,553	01/18/2000	Schneider, , et al.	714	21	01/26/1998
Dℑℛ	US-6,161,169	12/12/2000	Cheng, Danny T.	711	150	08/22/1997
Dℑℙ	US-6,272,651	08/07/2001	Chin, K. T., et al.	714	43	08/17/1998
Dℑℙ	US-6,310,815	10/30/2001	Yamagata, Tadato , et al.	365	230.03	08/07/1998

EXAMINER *Daniel Ryman*   **DATE CONSIDERED** 3 December 2003

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Examiner Name	Unknown
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DJR	US-6,363,502	03/26/2002	Jeddeloh, J.	714	52	07/22/1998
DJR	US-6,412,056	06/25/2002	Gharachorloo, K., et al.	711	202	10/01/1997
DJR	US-6,487,685	11/26/2002	Fiske, J A. S., et al.	714	701	09/30/1999
DJR	US-6,553,421	04/22/2003	Frick, John K., et al.	709	227	09/15/1998

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T^2
DJR	EP-0989484 A2	03/29/2000	Santahuhta, Raimo			

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T^2
DJR		Lattice Semiconductor Corporation, http://www.latticesemi.com,(2002),7 pgs.	
DJR		"Dynamic Datapath Selection for Unpredictable Transger Starts", IBM Technical Disclosure Bulletin, TBA-ACC-NO: NA9402589, Issue Number: 2A, Cross Reference: 0018-8689-37-2A-589,(1994),589-592	
DJR		"Dynamic Switch to Data Slow Mode on a Memory Card", IBM Technical Disclosure Bulletin, 37, NA9402637,(1994),321-322	
DJR		"Memory Card Data Fastpath", IBM Technical Disclosure Bulletin, 37, TDB-ACC-NO: NA9402637, Issue Number: 2A, Cross Reference: 0018-8689-37-2A-637,(1994),637-638	
DJR		"Synchronous External bus Architecture", IBM Technical Disclosure Bulletin, Jan. 1993, (01 01 93),104-107	
DJR		BREWER, KEVAN, "Re: Memory mapped registers", (Online): comp.arch.embedded, (05/02/96),	
DJR		GJESSING, et al., "Performance of the RamLink Memory Achritecture", Proceedings HICSS'94, (1994),154-162	
DJR		GJESSING, STEIN, et al., "RamLink: A High-BandwidthPoint-to-Point Memory Architecture", Proceeding CompCon, (1992),328/331	
DJR		IEEE STD, "IEEE Standard for High-Bandwidth Memory Interface Based on Scalable Coherent Interface(SCI) Signaling Technology (RAMLink)", IEEE Std 1596.4-1996, (1996),1-91	
DJR		RAO, A., "Memory mapped registers", new://comp.arch.ambedded, (04/27/96),	

EXAMINER Daniel Ryman   **DATE CONSIDERED** 3 December 2003